

## CLAIMS

We claim:

- 1     1. A memory system having a reduced refresh rate in a  
2     sleep mode, comprising:  
3         a dynamic memory;  
4         an error correction code (ECC) memory allocation  
5     circuit for identifying non-critical bit addresses in  
6     said dynamic memory and allocating said addresses as  
7     ECC addresses when entering from an active mode to  
8     sleep mode;  
9         an ECC encoder for encoding critical bits with  
10    error correction codes, said error correction codes  
11    being stored in said ECC addresses;  
12         a refresh execution circuit for reducing said  
13    refresh rate in said sleep mode and increasing said  
14    refresh rate in said active mode; and  
15         a ECC decoder for decoding said critical bits  
16    encoded with said error correction codes when  
17    reentering said active mode.
- 1     2. A memory system as recited in claim 1 further  
2     comprising a storage device for storing sleep mode  
3     refresh rate data.
- 1     3. A memory system as recited in claim 2 wherein said  
2     storage device comprises a fusible link.
- 1     4. A memory system as recited in claim 1 further  
2     comprising:  
3         a storage device for storing a plurality of sleep

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4 mode refresh rate data; and  
5 a temperature sensor, wherein said refresh  
6 execution circuit selects one of said sleep mode  
7 refresh rate data according to operating temperature.

1 5. A memory system as recited in claim 4 wherein said  
2 storage device comprises a fusible link.

1 6. A memory system as recited in claim 4 wherein said  
2 refresh rate is reduced by a 2X factor for each decade  
3 Celsius reduction in operating temperature.

1 7. A memory system as recited in claim 1 wherein said  
2 error correction codes comprises one of Reed-Solomon  
3 code and Bose-Chaudhuri-Hocquenghem code.

1 8. A memory system as recited in claim 1 wherein said  
2 ECC memory allocation circuit stores perallocated  
3 addresses in said dynamic memory.

1 9. A memory system as recited in claim 1 wherein said  
2 ECC memory allocation assigns ECC addresses dynamically  
3 to the last byte of each word address.

1 10. A method for reducing the refresh rate of a memory  
2 in sleep mode, comprising the steps of:  
3 switching from an active mode to a sleep mode;  
4 identifying non-critical bit addresses;  
5 encoding critical bits with an error correction  
6 code (ECC);  
7 storing ECC codes at said non-critical bit  
8 addresses;

9           reducing a refresh rate for said memory;  
10           performing error correction on said critical bits  
11       using said ECC codes when reentering active mode; and  
12           discarding said ECC bits.

1       11. A method for reducing the refresh rate of a memory  
2       in sleep mode as recited in claim 10 further comprising  
3       the step of:

4           determining an operating temperature for said  
5       memory; and

6           selecting one of a plurality of refresh rates  
7       based on said operating temperature of said memory.

1       12. A method for reducing the refresh rate of a memory  
2       in sleep mode as recited in claim 11 further comprising  
3       the step of:

4           reducing said operating temperature by a 2X factor  
5       for each decade Celsius reduction in operating  
6       temperature.

1       13. A method for reducing the refresh rate of a memory  
2       in sleep mode as recited in claim 10 further comprising  
3       the step of:

4           preallocating addresses in memory to store non-  
5       critical bits.

1       14. A method for reducing the refresh rate of a memory  
2       in sleep mode as recited in claim 10 further comprising  
3       the step of:

4           storing said ECC codes for a word at a last byte  
5       address for said word.

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1 15. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the  
3 refresh rate of a memory in sleep mode, the steps  
4 comprising:  
5 switching from an active mode to a sleep mode;  
6 identifying non-critical bit addresses;  
7 encoding critical bits with an error correction  
8 code (ECC);  
9 storing ECC codes in said non-critical bit  
10 addresses;  
11 reducing a refresh rate for said memory;  
12 performing error correction on said critical bits  
13 using said ECC codes when reentering active mode; and  
14 discarding said ECC bits.

1 16. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the  
3 refresh rate of a memory in sleep mode as recited in  
4 claim 15, the steps further comprising:  
5 reducing said operating temperature by a 2X factor  
6 for each decade Celsius reduction in operating  
7 temperature.

1 17. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the  
3 refresh rate of a memory in sleep mode as recited in  
4 claim 15, the steps further comprising:  
5 preallocating addresses in memory to store non-  
6 critical bits.

1 18. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the

3 refresh rate of a memory in sleep mode as recited in  
4 claim 15, the steps further comprising:  
5 storing said ECC codes for a word in a last byte  
6 byte address for said word.

1 19. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the  
3 refresh rate of a memory in sleep mode as recited in  
4 claim 15 wherein said error correction codes comprise  
5 Reed-Solomon code.

1 20. A computer readable medium embodying instructions  
2 for causing a computer to take steps to reduce the  
3 refresh rate of a memory in sleep mode as recited in  
4 claim 15 wherein said error correction codes comprise  
5 Bose-Chaudhuri-Hocquenghem code.

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